a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses.

4. (Amended) A frequency monitor, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor; and

a selector which, responsive to the indicator circuit output, selects from plural sources to control an oscillator.

11. (Amended) A frequency monitor, comprising:

a combiner circuit which combines two input signals to produce an error signal, the error signal having a frequency responsive to a difference between frequencies of the two input signals;

an edge detector which produces an output comprising a pulse for each rising/falling edge of the error signal;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor.

13. (Amended) A frequency lock system, comprising:

an oscillator which produces an output signal whose frequency is responsive to a control signal;

a frequency detector circuit which produces a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

an analog data phase detector circuit which produces a phase detector output signal that oscillates at a frequency responsive to the difference between the oscillator output signal's frequency and an input stream's data frequency;

a selector which selects one of the frequency detector output signal and the phase detector output signal as the control signal; and

a frequency monitor which controls the selector based on the frequency of the phase detector output signal.

17. (Amended) A method for monitoring frequency, comprising:

producing an output comprising a pulse for each rising/falling edge of the error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the error signal frequency; and

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount.

19. (Amended) A method for monitoring frequency, comprising:

producing an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the error signal frequency;

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount; and

selecting, responsive to the step of indicating, from plural sources to control an oscillator.

26. (Amended) A method for monitoring frequency, comprising:

combining two input signals to produce an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

producing an output comprising a pulse for each rising/falling edge of the error signal;

charging a capacitor to a charge responsive to the error signal frequency;

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount.

28. (Amended) A frequency lock method, comprising:

producing, from an oscillator, an output signal whose frequency is responsive to a control signal;

producing, from a frequency detector circuit, a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

producing, from an analog phase detector circuit, a phase detector output signal that oscillates at a frequency responsive to the difference between the oscillator output signal's frequency and an input stream's data frequency;

selecting one of the frequency detector output signal and the phase detector output signal as the control signal; and

controlling the selector with a frequency monitor.

30. (Amended) The method of Claim 28, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and input data frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

31. (Amended) The method of Claim 28, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and a reference clock frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

35. (Amended) A frequency lock system, comprising:

means for producing, from an oscillator, an output signal whose frequency is responsive to a control signal;

means for producing, from a frequency detector circuit, a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

means for producing, from an analog data phase detector circuit, a phase detector output signal that oscillates at a frequency responsive to the difference between the oscillator output signal's frequency and an input stream's data frequency;

means for selecting one of the frequency detector output signal and the phase detector output signal as the control signal; and

means for controlling said means for selecting based on the frequency of the phase detector output signal.

Please add new Claims 36-45.

36. (New) The frequency monitor of Claim 4, wherein the conductive circuit comprises:

a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses.

37. (New) The frequency monitor of Claim 4, wherein the indicator circuit comprises

a comparator that produces the indicator circuit output, said output being at one of two levels based on the charge and a threshold, a first level indicating that the difference between the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

38. (New) The frequency monitor of Claim 4, further comprising:

a combiner circuit which combines the two input signals to produce the error signal.

39. (New) The frequency monitor of Claim 38, wherein the combiner circuit comprises:

a mixer which mixes the two input signals to produce a mixed signal; and

a low-pass filter which filters the mixed signal to produce the error signal.

40. (New) The method of Claim 19, further comprising:

using a switched capacitor circuit to charge the capacitor, the switched capacitor circuit having an effective resistance that depends on error signal frequency.

41. (New) The method of Claim 19, further comprising:

combining the two input signals to produce the error signal.

42. (New) The method of Claim 41, wherein the step of combining comprises:

mixing the two input signals to produce a mixed signal; and

filtering, with a low-pass filter, the mixed signal to produce the error signal.

43. (New) The frequency monitor of Claim 11, wherein the conductive circuit comprises:

a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses.

44. (New) The frequency monitor of Claim 11, wherein the indicator circuit comprises:

a comparator that produces the indicator circuit output, said output being at one of two levels based on the charge and a threshold, a first level indicating that the difference between the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

45. (New) The method of Claim 26, further comprising:

using a switched capacitor to charge the capacitor, the switched capacitor having an effective resistance that depends on error signal frequency.